Docket No. 500.30310CX2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Nobuo HAMAMOTO *et al.*

Serial No.: Unassigned (§53b Continuation of 08/446,278)

Filed: 22 June 2001

For: DIGITAL INFORMATION SYSTEM, DIGITAL AUDIO SIGNAL PROCESSOR AND SIGNAL CONVERTER

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231 22 June 2001

Sir:

Prior to calculating the filing fee for the above-identified application, the following amendments and remarks are respectfully submitted.

IN THE SPECIFICATION:

Page 1, between the title and line 1 ("BACKGROUND OF THE INVENTION"), please insert the following new section.

--CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of Serial No. 08/446,278 filed 22 May 1995, now allowed, which is a continuation of Serial No. 07/727,420 filed 9 July 1991, abandoned.--

IN THE CLAIMS:

Please cancel claims 1-45 as originally filed, and substitute therefor replacement claims 46-54, as follows.

46.(New) A memory apparatus having a playback function removably connected with a digital signal source to store digital data received from said digital signal source and to reproduce the digital data stored therein independently of said digital signal source, comprising:

a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of said digital data from said digital signal source; and

a built-in playback circuit, including a digital-to-analog converter, a filter circuit and an audio amplifier, for reproducing digital data stored in said memory circuit.

47.(New) A memory apparatus according to Claim 46, wherein said digital data is transmitted by communication means.

48.(New) A memory apparatus according to Claim 46, wherein said built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code.

49.(New) A memory apparatus according to Claim 46, wherein said memory apparatus is a card-like storage medium.

50.(New) A memory apparatus according to Claim 46, wherein said playback circuit has playback conditions which include stereo or monaural playback, a resolution of 8 and 16 bits, and a sampling frequency.

51.(New) A memory apparatus having a playback function removably connected with a digital signal source to store digital data received from said digital signal source and to reproduce the digital data stored therein independently of said digital signal source, comprising:

a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of said digital data from said digital signal source;

a built-in playback circuit, including a digital-to-analog converter, a filter circuit and an audio amplifier, for reproducing digital data stored in said memory circuit; and

a rechargeable battery capable of being charged by a power supply in said digital signal source when said memory card is connected with said digital signal source.

52.(New) A memory apparatus according to Claim 51, wherein said built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code.

53.(New) A memory apparatus according to Claim 51, wherein said memory apparatus is a card-like storage medium.

54.(New) A memory apparatus according to Claim 51, wherein said playback circuit has playback conditions which include stereo or monaural playback, a resolution of 8 and 16 bits, and a sampling frequency.

IN THE ABSTRACT:

Please delete the ABSTRACT OF THE DISCLOSURE as originally filed, and substitute therefor the following replacement Abstract.

--ABSTRACT OF THE DISCLOSURE

A digital information system for sale of information in the form of digital signals, and an audio processor, a data compressor, a data extender and a signal processor suitably used with the system. When a digital signal is received, a digital signal source is connected directly to a player for receiving and storing a specified information, which is reproduced by the player independently. A voice interval of a digital audio signal is processed for slow and fast playback. The fast and slow playback are possible without deteriorating the sound quality, and ripples can be greatly reduced against the digital input signal, thereby making possible a faithful data compression of an acoustic signal or the like by a simple configuration. The self-diagnosis function permits the use of a defective memory chip, thereby leading to a very economical system.--

REMARKS

Applicants respectfully request consideration of the following information.

AMENDMENTS

The specification initially has been amended to incorporate information regarding related applications for which benefit of an earlier filing date is relied upon in the present continuation application. Applicants reserve the right to present

supplemental Preliminary Amendments to amend the specification as necessary to conform it to U.S. practice and to correct minor grammatical and idiomatic inconsistencies therein, as were submitted and entered in the parent application.

The Abstract has been amended to conform it to U.S. practice requirements for a length of 50-150 words.

Approval and entry of the amendments are courteously solicited.

PENDING CLAIMS

Original Claims 1-45 have been cancelled, and new Claims 46-54 are submitted herewith. No new matter is added, and all of the limitations in the new claims find full support and antecedent basis in the original application as filed. Therefore, upon entry of this Preliminary Amendment, Claims 46-54 will be pending for examination and consideration in the present continuation application.

DRAWING CHANGES

Filed concurrently herewith is a Letter to the Official Draftsperson with proposed figure corrections shown in highlight, which are identical to those required and entered in the parent application. No new matter is added.

Also, attached hereto are forty-six (46) sheets of formal drawings for Figures 1-69 with the highlighted proposed drawing corrections completed thereon. Therefore, approval and entry of the proposed drawing corrections are respectfully requested.

INFORMATION DISCLOSURE STATEMENT

Filed concurrently herewith is an Information Disclosure Statement and Form PTO-1449 to identify all of the art cited to or by the Office in the parent applications, for entry in the present application so they appear on the printed face of any patent issuing hereon.

PRIORITY

Applicants claim priority under 35 U.S.C. §119 of JP 02-181402 filed 11 July 1990, JP 02-208072 filed 8 August 1990, JP 03-057972 filed 27 February 1991, and JP 03-057930 filed 28 February 1991. Certified copies of the priority documents and certified copies of English-language translations therefor were filed and acknowledged in prior application Serial No. 07/ 727,420. Confirmation of perfection of Applicants' claim for priority in the present application is courteously solicited.

ASSIGNEE OF FULL TITLE

Hitachi, LTD. is Assignee of full right, title and interest in and to the present case by virtue of the Assignment filed in prior application Serial No. 07/727,420 and recorded 9 July 1991 at Reel 5168, Frames 997-999.

APPENDIX A-MARKED VERSION

Attached to this Preliminary Amendment is Appendix A-Marked Version showing the amendments made herein by bracketing and underlining of deletions and additions, respectively.

CONCLUSION

This Preliminary Amendment is being filed concurrently with the present continuation application, and therefore, no additional fee is required.

Please charge any deficiencies in the fees filed herewith to ATS&K Deposit Account No. 01-2135 (as Order No. 500.31310CX2), and credit any overpayment thereto.

Respectfully submitted,

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ANTONELLI, TERRY, STOUT & KRAUS
1300 North Seventeenth Street, Suite 1800
Arlington, VA 22209
Telephone 703-312-6600
Facsimile 703-312-6666

ATTACHMENTS:

- Appendix A-Marked Version
- IDS/Form PTO-1449
- Letter to Official Draftsperson and Drawing Corrections
- Eighteen (18) sheets of formal drawings (Figs. 1-69)

APPENDIX A-MARKED VERSION

ABSTRACT OF THE DISCLOSURE

[In a] A digital information system for [realizing the] sale of information [or the like having a commercial value] in the form of [a] digital [signal] signals, and an audio processor, a data compressor, a data extender and a signal processor suitably used with the system[, when]. When a digital signal is received[/delivered], a digital signal source is connected directly to a player for receiving and storing a specified information, which is reproduced by the player independently. A voice interval of a digital audio signal is processed [to realize the] for slow and fast playback. [The system includes a data compressor and a data extender of a simple configuration. The value of the digital signal received/delivered can be exhibited directly. A selling system is constructed easily, and the player is simple in configuration and easy to operate by anyone.] The fast and slow playback are possible without deteriorating the sound quality, and ripples can be greatly reduced against the digital input signal, thereby making possible a faithful data compression of an acoustic signal or the like by a simple configuration. The self-diagnosis function permits the use of a defective memory chip, thereby leading to a very economical system.

FIG. 1

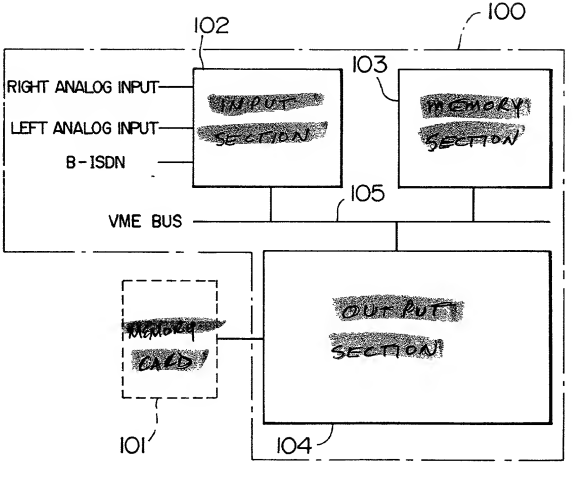

100
102
103
RIGHT ANALOG INPUT
LEFT ANALOG INPUT
B-ISDN
INPUT SECTION
MEMORY SECTION
105
VME BUS
MEMORY CARD
OUTPUT SECTION
101
104

FIG. 2

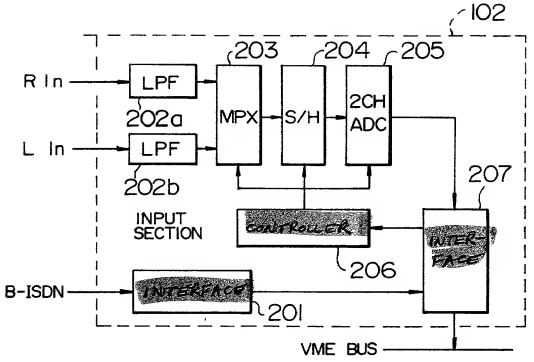

102
203
204
205
R In
LPF
202a
MPX
S/H
2CH
ADC
L In
LPF
202b
207
INPUT
SECTION
CONTROLLER
INTER-
FACE
206
B-ISDN
INTERFACE
201
VME BUS

FIG. 3

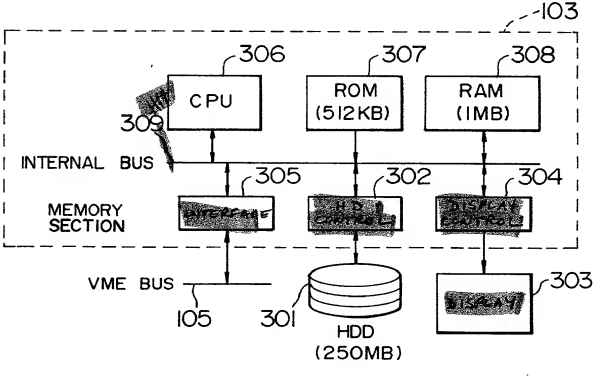

103
306
307
308
CPU
ROM
(512KB)
RAM
(1MB)
309
INTERNAL BUS
305
302
304
MEMORY
SECTION
INTERFACE
H.D.
CONTROLLER
DISPLAY
CONTROLLER
VME BUS
105
301
HDD
(250MB)
303
DISPLAY

FIG. 4

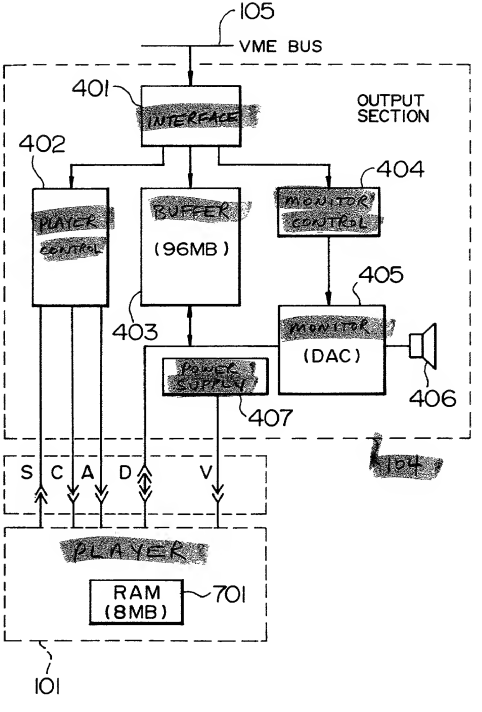

105
VME BUS
401
INTERFACE
OUTPUT SECTION
402
404
PLAYER CONTROL
BUFFER
(96MB)
MONITOR CONTROL
405
403
MONITOR
(DAC)
406
POWER SUPPLY
407
104
S
C
A
D
V
PLAYER
RAM
(8MB)
701
101

FIG. 5

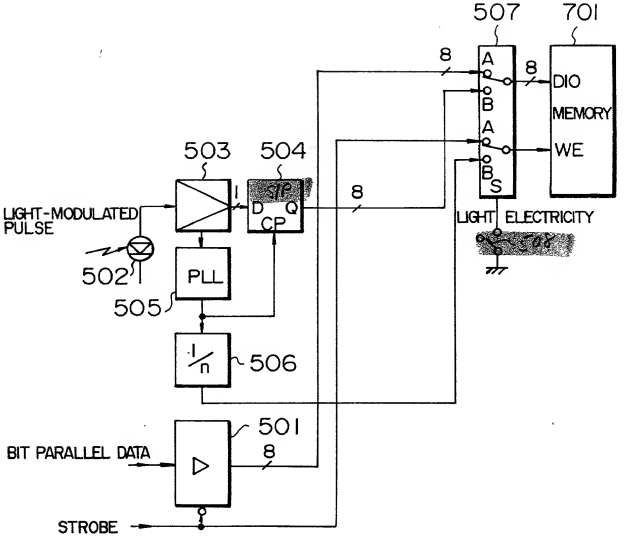

507
701
8
A
B
A
B
S
8
DIO
MEMORY
WE
503
504
I
D
Q
CP
8
LIGHT-MODULATED PULSE
LIGHT ELECTRICITY
502
PLL
505
1/n
506
501
BIT PARALLEL DATA
8
STROBE

FIG. 6

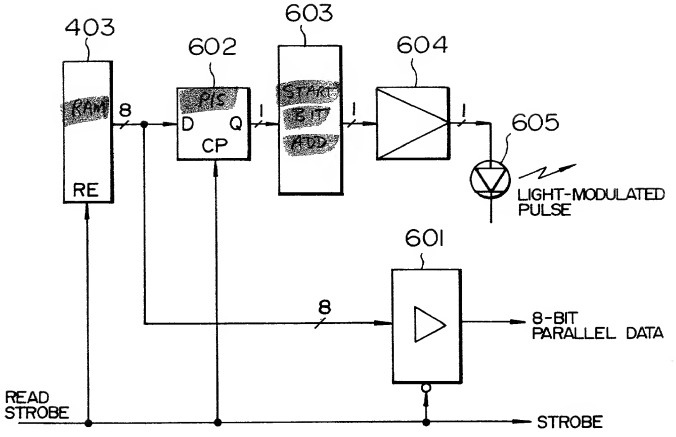

403
602
603
604
605
601
RAM
RE
8
D
Q
CP
1
1
1
8
8
8-BIT
PARALLEL DATA
LIGHT-MODULATED
PULSE
READ
STROBE
STROBE

FIG. 7

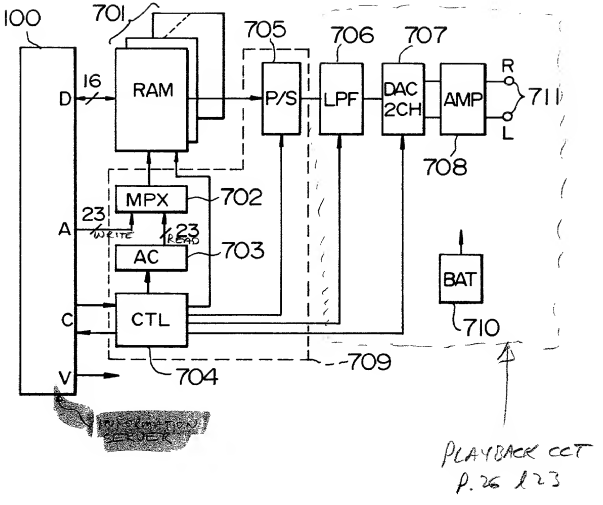

100
701
705
706
707
16
D
RAM
P/S
LPF
DAC
2CH
AMP
R
L
711
MPX
702
23
WRITE
23
READ
A
AC
703
BAT
710
C
CTL
704
709
V
708
PLAYBACK CCT
P. 26 l 23

FIG. 30

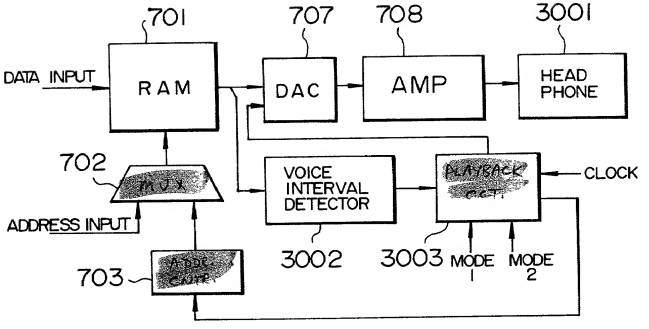

701
707
708
3001
DATA INPUT
RAM
DAC
AMP
HEAD PHONE
702
MUX
VOICE INTERVAL DETECTOR
PLAYBACK CNTR
CLOCK
ADDRESS INPUT
ADDR CNTR
703
3002
3003
MODE 1
MODE 2

FIG. 31

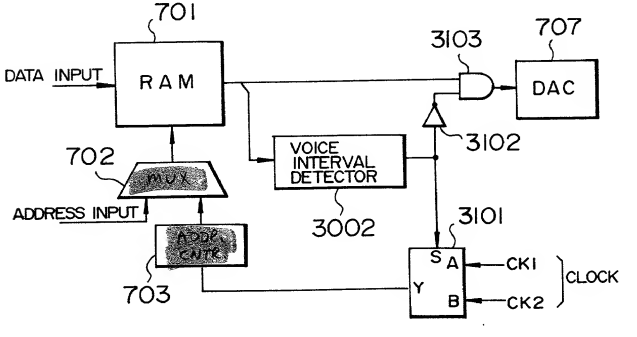

701
3103
707
DATA INPUT
RAM
DAC
3102
702
MUX
VOICE INTERVAL DETECTOR
ADDRESS INPUT
3002
3101
ADDR CNTR
S
A
CK1
CLOCK
Y
B
CK2
703

FIG. 32

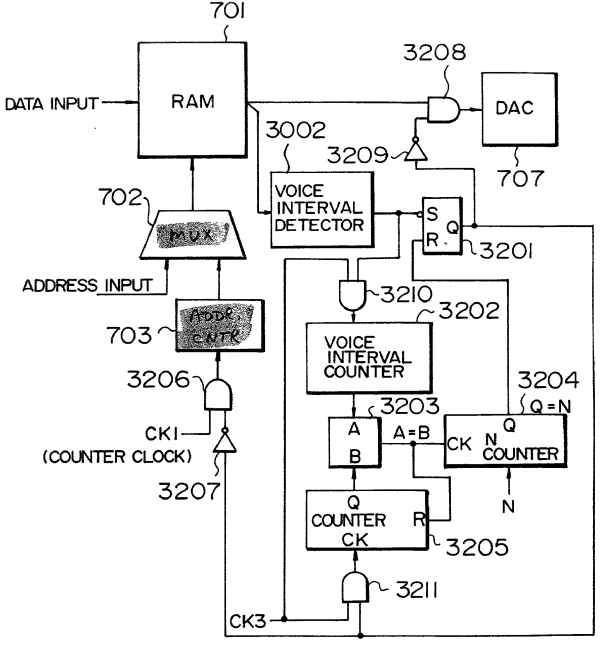

701
RAM
DATA INPUT
3208
DAC
707
3002
3209
VOICE INTERVAL DETECTOR
S
Q
R
3201
702
MUX
ADDRESS INPUT
3210
3202
703
ADDR CNTR
VOICE INTERVAL COUNTER
3206
3204
Q=N
3203
CK1
(COUNTER CLOCK)
A
B
A=B
CK
N
Q
COUNTER
3207
N
Q
COUNTER
CK
R
3205
3211
CK3

FIG. 35

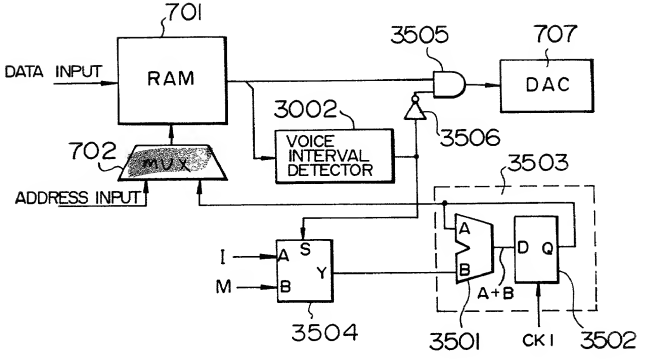

701
3505
707
DATA INPUT
RAM
DAC
3002
VOICE INTERVAL DETECTOR
3506
702
MUX
3503
ADDRESS INPUT
A
D Q
B
A+B
I
M
A S
B
Y
3504
3501
CK1
3502

FIG. 36

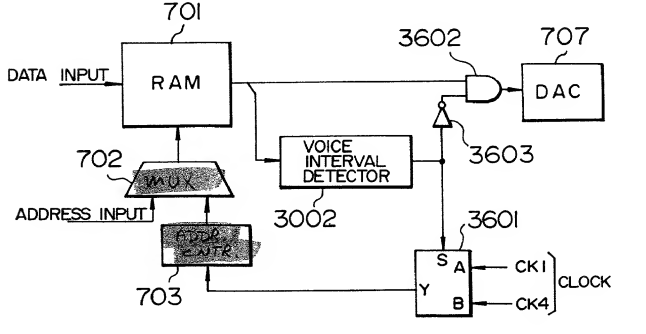

701
3602
707
DATA INPUT
RAM
DAC
3603
VOICE INTERVAL DETECTOR
702
MUX
ADDRESS INPUT
3002
3601
703
S A
Y
B
CK1
CK4
CLOCK

FIG.37

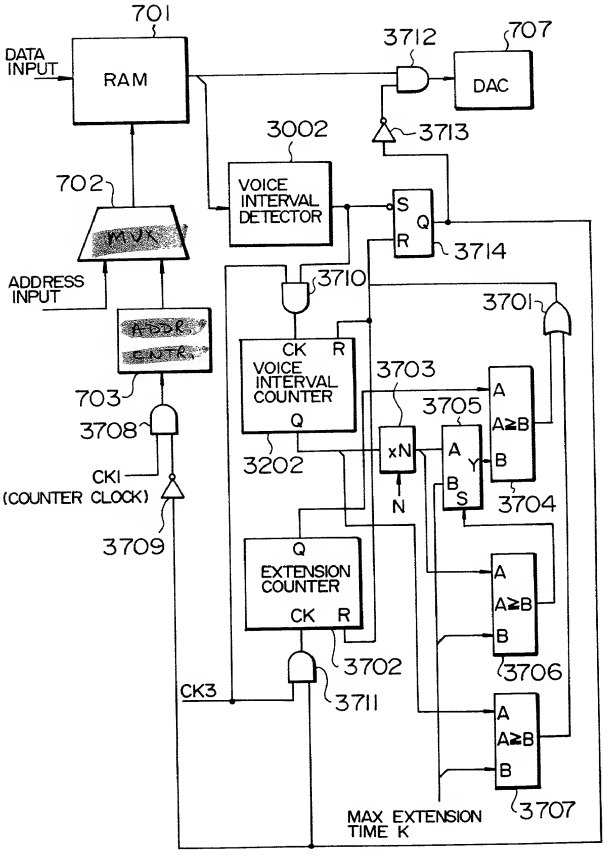

701
DATA INPUT
RAM
3712
707
DAC
3713
3002
VOICE INTERVAL DETECTOR
S
Q
R
3714
702
MUX
ADDRESS INPUT
3710
3701
ADDR
ENTR
CK R
VOICE INTERVAL COUNTER
Q
3703
703
3708
3705
A
A≥B
B
xN
A
Y
B
S
N
3704
3202
CKI
(COUNTER CLOCK)
3709
Q
EXTENSION COUNTER
CK R
3702
3706
CK3
3711
3707
MAX EXTENSION TIME K

FIG. 43

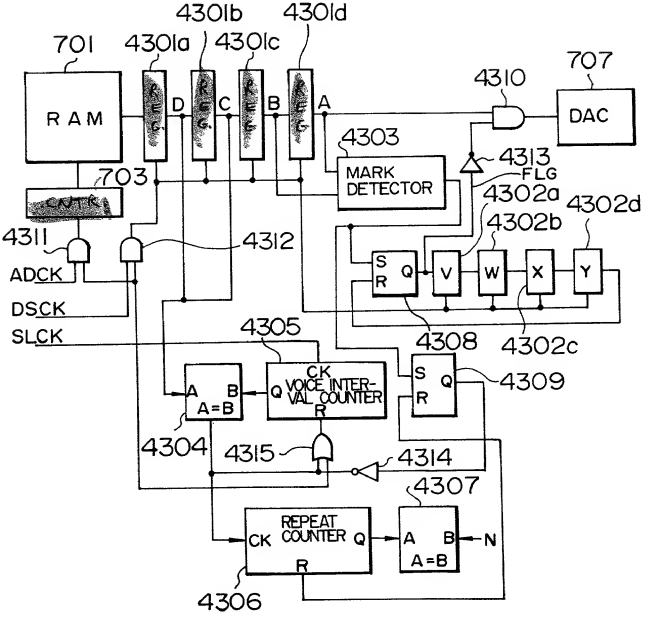

4301b
4301d
701
4301a
4301c
707
4310
RAM
D
C
B
A
DAC
4303
4313
MARK DETECTOR
FLG
703
4302a
4302d
4302b
4311
4312
S
R
Q
V
W
X
Y
ADCK
DSCK
SLCK
4305
4308
4302c
CK
VOICE INTER-VAL COUNTER
A
B
A=B
S
R
Q
4309
4304
4315
4314
4307
REPEAT COUNTER
CK
Q
A
B
A=B
N
4306

FIG. 44

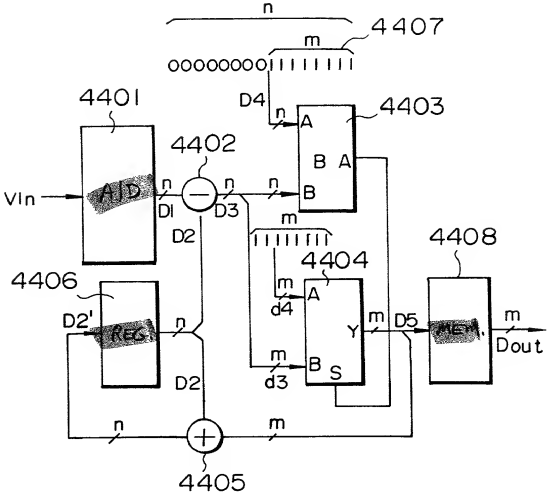

n
4407
m
4401
D4
4403
4402
A
B A
Vin
A/D
n
n
n
B
DI
D3
m
D2
4408
4404
4406
m
A
d4
D2'
REG
n
m
Y
m
D5
m
Dout
m
B
S
d3
D2
n
m
4405

FIG. 45

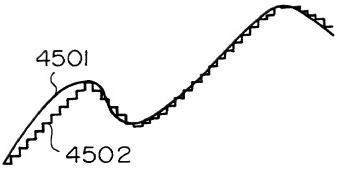

4501
4502

FIG. 46

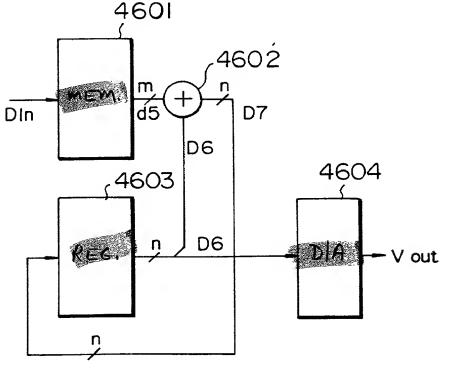

4601
4602
MEM.
m
n
DIn
d5
D7
D6
4603
4604
REG.
n
D6
D/A
V out
n

FIG. 47

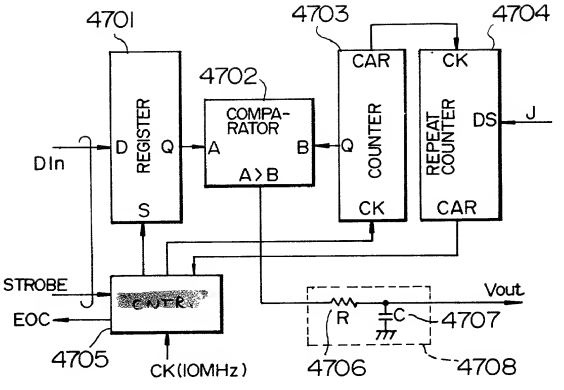

4701
4703
4704
4702
CAR
CK
COMPA-
RATOR
REGISTER
COUNTER
REPEAT
COUNTER
DS
J
DIn
D
Q
A
B
Q
A>B
S
CK
CAR
STROBE
EOC
Vout
R
C
4707
4705
CK(10MHz)
4706
4708

FIG. 48

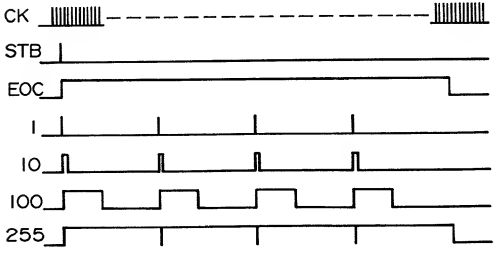

CK
STB
EOC
1
10
100
255

FIG. 50

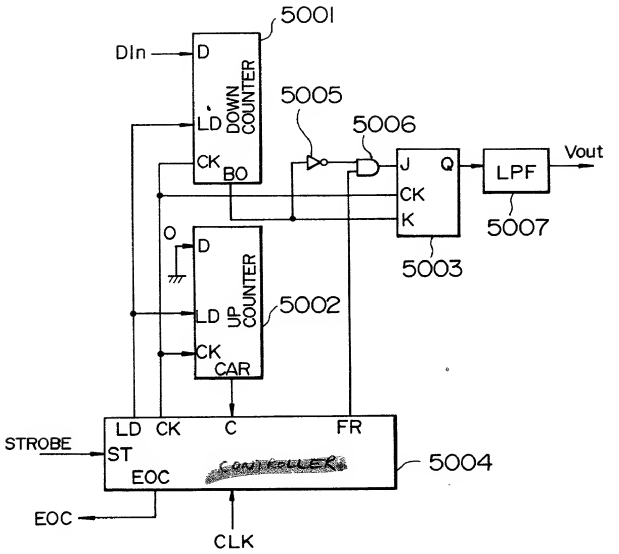

5001
DIn
D
DOWN COUNTER
LD
CK
BO
5005
5006
J
Q
CK
K
LPF
Vout
5007
5003
0
D
UP COUNTER
LD
CK
CAR
5002
LD
CK
C
FR
STROBE
ST
EOC
CONTROLLER
5004
EOC
CLK

FIG. 56

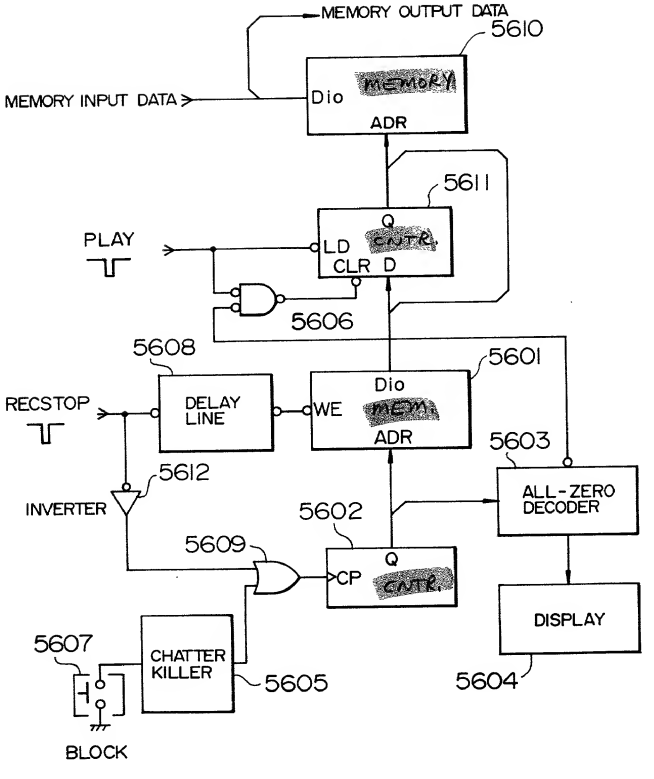

MEMORY OUTPUT DATA
5610
MEMORY INPUT DATA
Dio
MEMORY
ADR
5611
Q
CNTR.
PLAY
LD
CLR
D
5606
5608
5601
RECSTOP
DELAY LINE
WE
Dio
MEM.
ADR
5603
5612
INVERTER
5602
ALL-ZERO DECODER
5609
Q
CP
CNTR.
DISPLAY
5607
CHATTER KILLER
5605
5604
BLOCK

FIG. 59

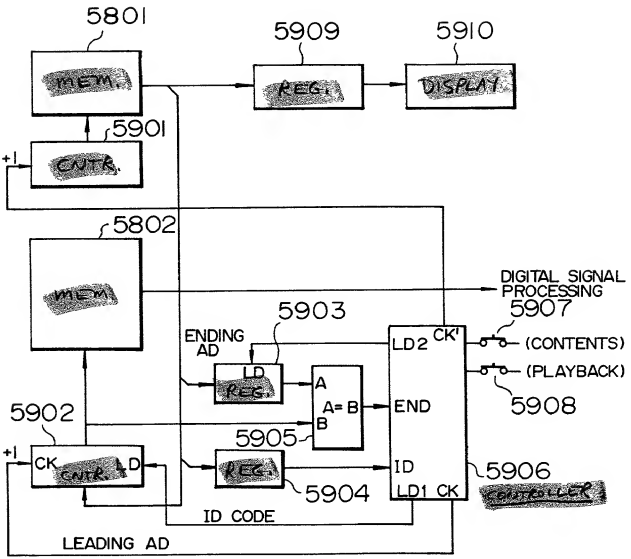
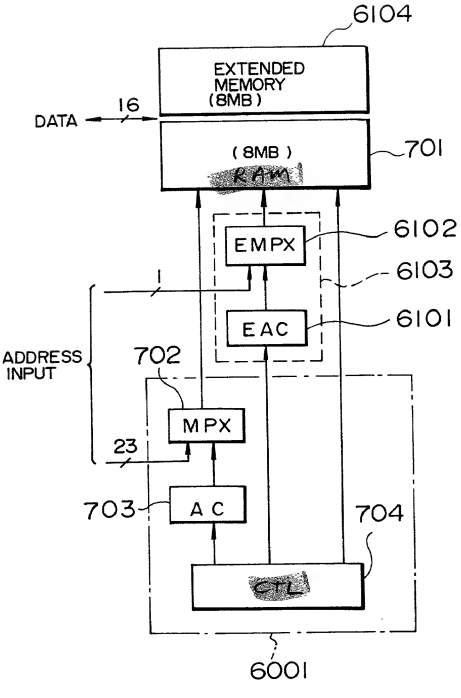

5801
MEM.
5909
REG.
5910
DISPLAY
5901
CNTR.
+1
5802
MEM.
DIGITAL SIGNAL PROCESSING
5907
(CONTENTS)
(PLAYBACK)
5908
5903
ENDING AD
LD
REG.
A
A=B
B
LD2
CK'
END
5902
5905
+1
CK
CNTR.
LD
REG.
ID
LD1
CK
5906
CONTROLLER
5904
ID CODE
LEADING AD

FIG. 61


6104
EXTENDED MEMORY (8MB)
DATA
16
(8MB)
701
EMPX
6102
6103
EAC
6101
ADDRESS INPUT
702
MPX
23
703
AC
704
6001